

Reducing HDI Via-in-Pad Solder Joint Voids with a Simple Copper Viafill

Chrys Shea, Alpha Metals N.J. USA | David Ormerod, Enthone Inc. CT USA

Introduction

High Density Interconnect designs are being relentlessly driven by the mass market competition and rapidly evolving development of handheld and other electronic devices. Leading the charge are portable electronic products like mobile phones, personal digital assistants and music players. Such designs continue to place growing demands on the performance and resultant reliability of both the PWB Fabrication and Assembly processes. Blind-microvia and via-in-pad designs have become the standard to save on precious real estate. This HDI trend is being further enabled by micro-via sizes dipping below 100 microns diameter and now approaching and ultimately surpassing 50 microns. Corresponding aspect ratios are also trending from 1:1 to 0.75 and below. For some companies, the concerns of such higher complexity designs, expensive performance qualification tests, and lower assembly yields have challenged their adoption due to fears of low yields and increased product costs. For the Fabricator, it has become a genuine challenge to plate these microvia features reliably (copper PTH and final finish) and finally to keep them free from moisture and corrosion products. The assemblers, already challenged by the impact of Lead-free soldering requirements, are looking to effectively eliminate sources of contamination, unwanted solder joint voids and planarity variation.

The ODMs and OEMs have increasingly recognized the benefits of copper-filled micro-vias which include: the elimination the macro-voiding in solder joints on via-in pad designs; the improved thermal relief and the 'known CTE'. As a result, this approach is being more broadly applied in new designs. With the ability of copper via fill to eliminate the previously described fabrication and assembly issues, the wider application of filled vias provides an opportunity for a 3 way improvement synergy for the supply chain.

There are various approaches to fill such micro-vias and better data is now arising which confirms the beneficial impact of copper via-fill electroplating. However, one legitimate concern from the fabricator is the cost and complexity of employing any additional processes for the selective plating of these features. However, this is not necessarily required. This article reviews one simple electroplating approach for copper via-fill, which can be "dropped-in", and which is capable of plating both through-hole and filled features simultaneously. The resulting performance is supported by some test studies at the assembly level, which underpins the established benefits from both fabrication and assembly points of view.

Problems associated with Unfilled Blind Microvias

On the assembly side, blind microvias present a unique set of challenges. It has been documented that small discrete components like 0402s or 0201s can deplete solder from the joint being formed, raising reliability concerns. A broader concern, however, is the issue of solder joint-voiding when microvias are in the pads of area array devices, like microBGA-style components. Figure 1 shows a cross section of such an area array device with microvias in every pad. Considerable voiding is observed in these joints. Such large voids occur because the cavity in the pad surface entraps air during the solder paste printing portion of the assembly process.

On the plating front, using conventional PWB fabrication processes and equipment, a blind microvia size of 2 mils (50 microns) or even 4 mils (100 microns) can present significant challenges with regard to wetting, PTH plating, Final-Finishing and many other processing steps. The following types of defects have been known to result:

- Breakdown in the continuity of the base copper

metallization (voids). Often caused by poor solution penetration/turnover within the vias or gassing within the electroless copper process.

- Incomplete coverage of the final surface finish due to contamination or poor solution dynamics.
- Voiding due to etch out of the electroplated copper as a result of incomplete or porous electrolytic tin etch resist coverage
- Entrapped water and/or corrosive process chemistries resulting from poor rinsing and drying in several processes.

Some examples of processing challenges and problems arising are show in Figure 2.

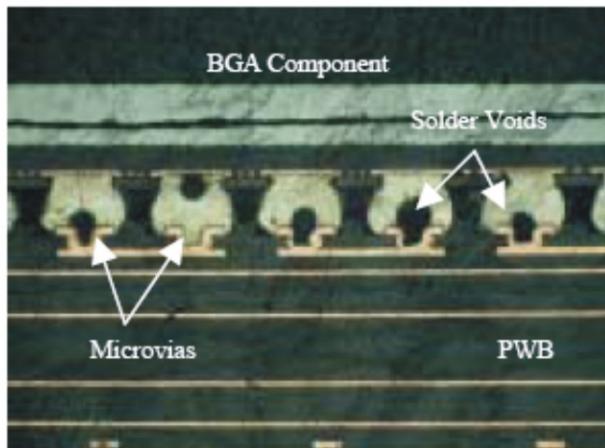


Figure 1. Microvia induced solder voids

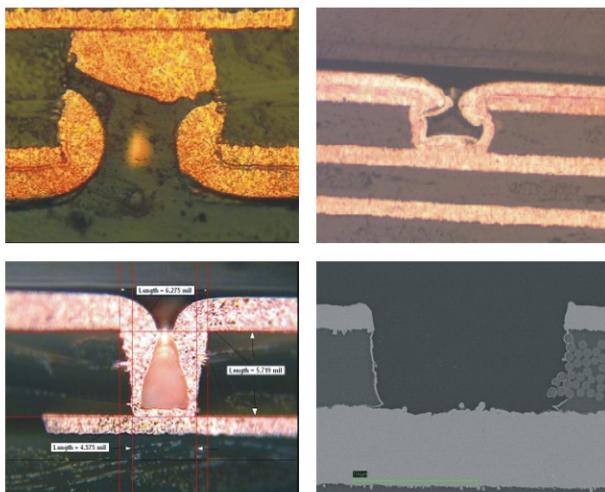


Figure 2. Plating Challenges for Micro-vias

The correlation of void size to the reliability of BGAs is a contentious issue within the assembly

community. Most assemblers avoid the debate but subscribe to the position of: The smaller and fewer the voids, the better. A print-reflow process that exhibits maximum void size rates typically in the neighborhood of five percent can see that number rise dramatically to twenty-five percent or higher when microvias in pads are introduced. About 5% of this can be attributed to the solder paste but the remaining 20% comes from the micro-via itself. Such numbers can be very alarming to the engineering team regardless of their general position on void size and reliability! The retention of entrapped moisture or residual contaminants in these relatively inaccessible blind via-holes, during or especially after the fabrication process, can provide additional contributions to void formation or event joint failure. The extremely hot soldering conditions causing rapid release into the melting solder paste.

Even if the microvias are clean and dry, the voiding issues from microvia-in-pad designs, encountered at board-level assembly, are not influenced by the type of final solderable finish of the PWB. Voiding is seen with all finishes, but not always in the same position. For example, with copper OSP finishes, the low rate of spread of lead-free solders results in voids, which do not move within the solder joint, leaving the trapped air in its original location within the microvia. By contrast, the higher rates of solder spread of the same lead-free alloy on an Electroless Nickel / Immersion Gold finish (ENIG) helps to liberate the trapped air into the bulk of the joint. Figure 3 shows similar 0.5mm pitch CABGA solder joints with unfilled 100 micron vias in their pads. The one on the left has an OSP final finish; the one in the center has an ENIG final finish. These are compared with a copper via-filled pad on the right (with no void). It is arguable that while the general opinion leans toward a preference for containing the void within the via, as seen on the OSP finish, the optimal approach must be to eliminate it completely!

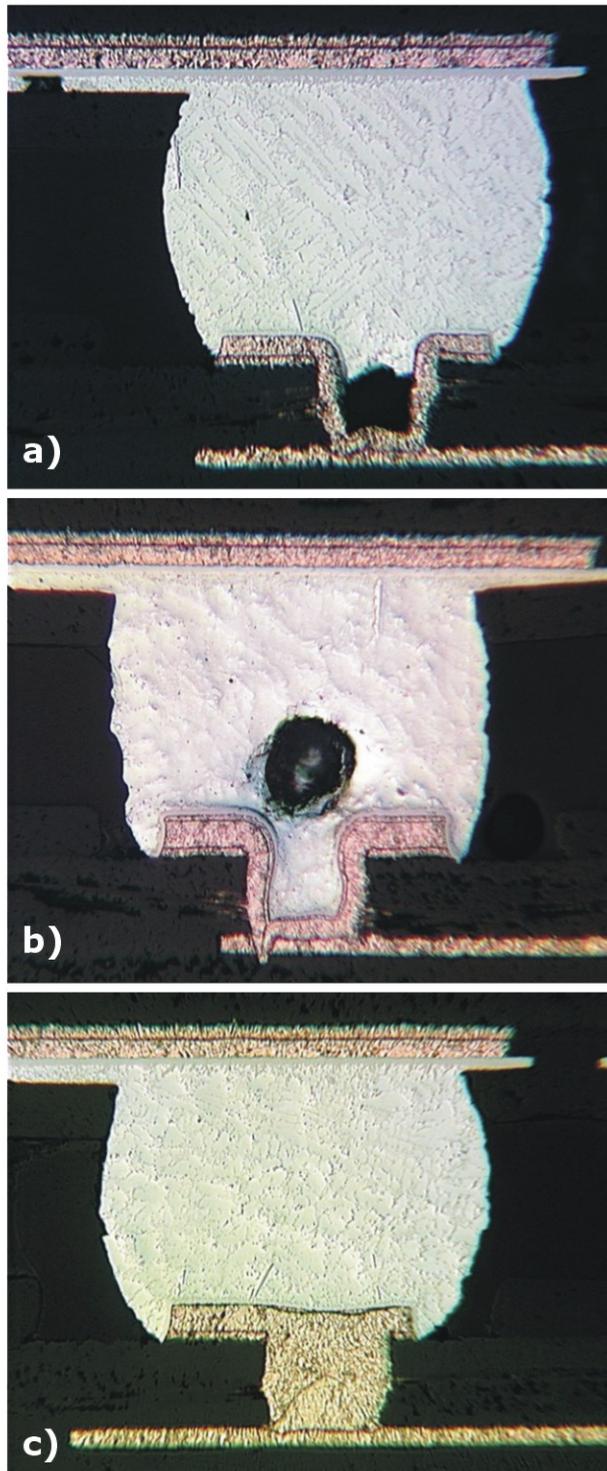


Figure 3. BGA solder joints with unfilled microvias on an OSP finish (a); on an ENIG finish (b) and with a filled via (c).

One escalating problem here, as dimensions reduce, relates to the microvias in smaller pads which can produce very large voids in very small solder joints.

Approach to Eliminating Solder Joint Voids

The good news is that there are relatively simple solutions at hand. A range of via-filling technologies are available to the fabricator. These include:

- a) Inorganic Thick Film Pastes;
- b) Organic pastes including unfilled, metal filled and inorganic filled types
- c) Electrolytic Copper Plated Via-Fill

It is clear that all these via-fill methods can improve structural integrity and provide varying degrees of enhanced thermal relief. However, the paste-based processes are typically better suited to larger through-hole vias (>10mils or 0.25mm diameter). By contrast, the processes which use electroplated plated copper are better suited for smaller, blind micro-vias (<7 mils or <175microns diameter). The electrolytic copper-filling of vias benefits design performance by: improving thermal conductivity; providing a known coefficient of thermal expansion (CTE) aligned with the board metallization; and by readily supporting "stacked via" designs. There are additional benefits for the fabricator as some of the available copper via fill processes offer conformal plating of the through holes (PTH) while simultaneously achieving complete filling of the microvias. This removes any unwanted, additional process steps associated with paste filling processes. For the assembler, the elimination of the small, deep, air-trapping wells on the pad surfaces renders soldering performance similar to that of planar pads and the issue of excessive voiding is practically eliminated.

Approaches to Electrolytic Copper Via-filling

It is readily possible to perform copper via-filling as a second plating operation using custom designed plating additives to promote low current density deposition. However, such an approach requires the additional plating step using additional vertical or horizontal equipment, and likely demands a selective dry film process. Such processes may run using either soluble copper anodes or inert anodes in conjunction with DC or periodic pulse reverse

(PPR) rectification. The disadvantages here are the additional capital costs, process steps and increased process "cost of ownership" including additional water and utilities.

However, there is a simpler and more cost-effective alternative approach for the fabricator using a technology that plates through-holes while simultaneously filling the blind microvias. This approach is a simple one that drops into existing vertical electrolytic plating lines using soluble copper anodes. The concept and application are described as follows:

Simple Copper Via-fill Process

Conventional Electrolytic copper baths, based on a sulfuric acid-copper sulfate, typically contain additive systems, which incorporate an activator and a suppressor, plus other components. These components control not only the deposition characteristics of the copper but also directly impact the physical properties of the deposit. They are dosed into the single step bath at very low concentrations and are typically more difficult to measure. The analysis involves the use of more complex CVS (Cyclic Voltammetric Stripping) techniques to measure the multiple components. Control is very important as excess build-up of the additives, or their breakdown products, can cause embrittlement and stress cracking of the copper deposit.

By contrast, the copper process utilized in this study does not contain any activator in the electrolytic step. Instead, the proprietary¹ process actually works on a simple 2 step system where the PWBs are first pre-dipped in an activator bath before transferring to the plating cell that contains the suppressor. Ultrasonic energy or vibration is applied to ensure that the accelerator penetrates and concentrates within all the small blind microvia features. The PWBs are then transferred to the electrolytic plating cell and, at the start-up of the plating cycle, the activator (already concentrated in the lower current density areas) selectively drives the deposition within the blind microvia recesses. As plating progresses, the larger and slower moving suppressor molecules restrict any excessive and

unwanted copper deposition on the panel outer-surfaces, which results in fast and efficient filling of the microvias. The use of the two separate baths makes the CVS control much simpler and more precise. Additionally, the total organic levels in the plating bath are moderated, therefore improving the physical integrity of the copper deposit and its resistance to cracking under thermal shock conditions. This is critical for any process which plates through-holes as well as microvias. The copper deposited by this process meets and exceeds all the standard deposit performance test requirements for through-hole metallization, showing typical elongation values of 28% and tensile strengths of 44,000 psi (304 N/mm²). These values are well in excess of IPC-6012B minimums, which are cited as 12% elongation and 36,000 psi (248 N/mm²).²

This simple 2 step process is operated in a standard, vertical DC, air agitated plating cell, thereby eliminating the need for any specialized equipment⁸. The process sequence is shown in figure 4 and a schematic diagram of the via-filling mechanism in figure 5.

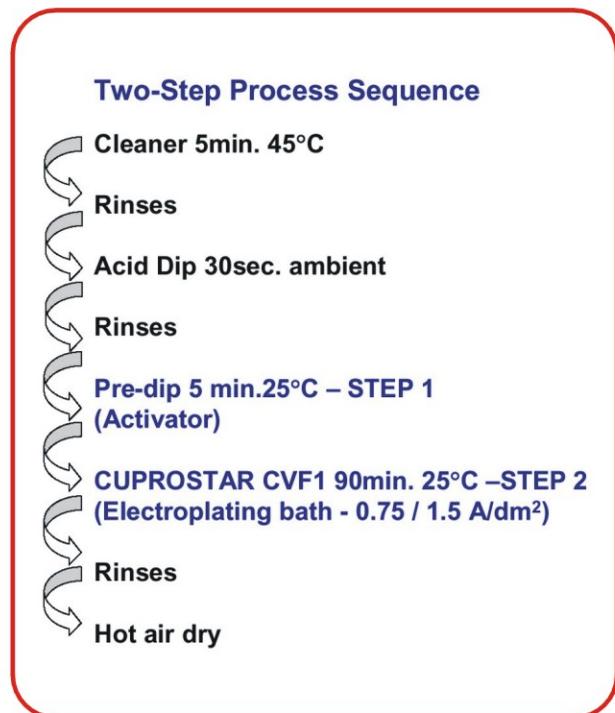


Figure 4. Viafill Process Sequence

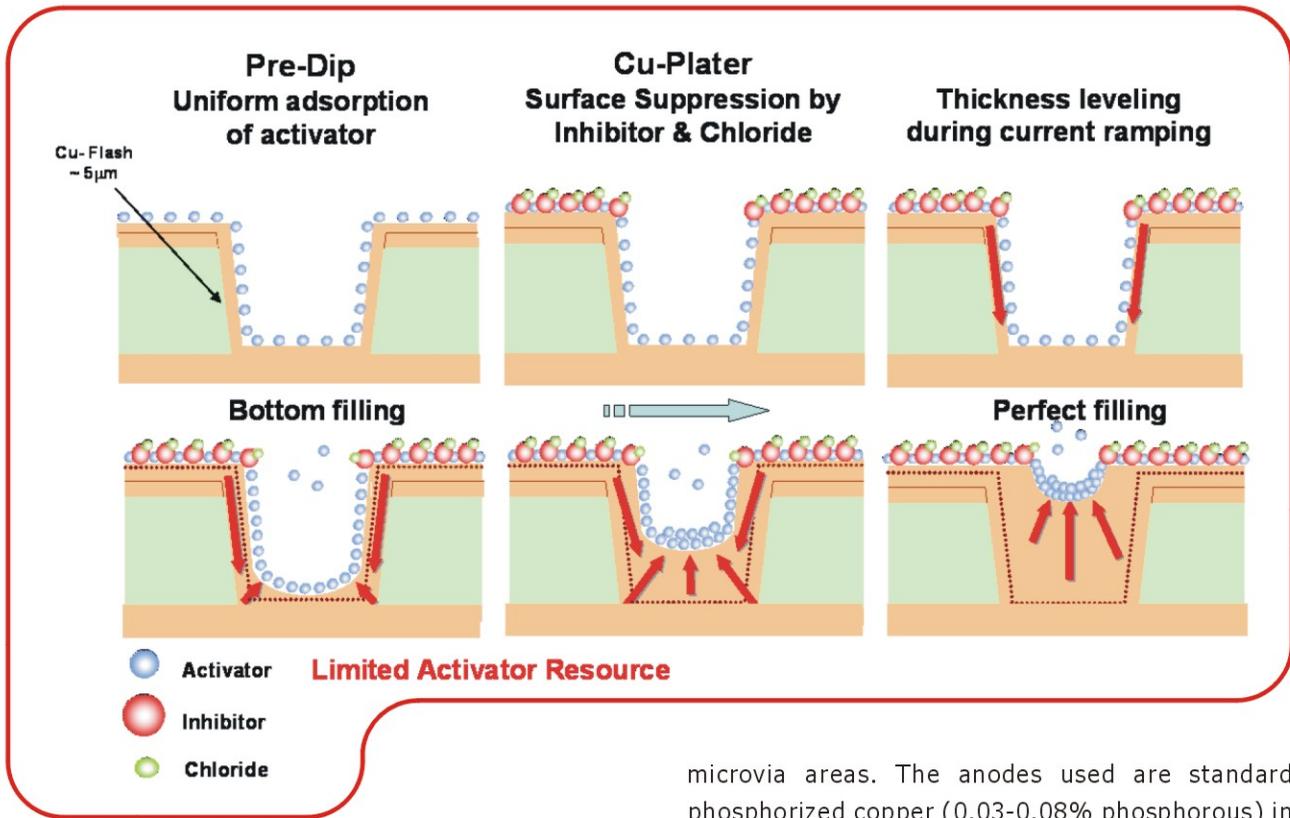


Figure 5. Simple 2-step Via filling mechanism

Whereas the electrolyte for standard PTH copper normally operates at 20-25 g/L copper and 180-220 g/L Sulphuric acid, the Copper Via Fill (CVF) process described utilizes typically 50 g/l Copper as Cu^{2+} , 100 g/l H_2SO_4 , 70 mg/l Cl^- and 1.0 ml/l CVF inhibitor. This facilitates much more effective copper deposition in the inaccessible low CD

microvia areas. The anodes used are standard phosphorized copper (0.03-0.08% phosphorous) in basket or bar form. The plating sequence is nominally 15 minutes at 0.75 Amps/dm^2 (7 Amps/ft^2) followed by a ramp up to $1.5-1.9 \text{ Amps/dm}^2$ ($14-18 \text{ Amps/ft}^2$) for 60-90 minutes, depending on the microvia depths and aspect ratios. The use of the step-ramped current⁷ ensures that the initial copper deposition along the via hole walls enhances the plating current distribution to the

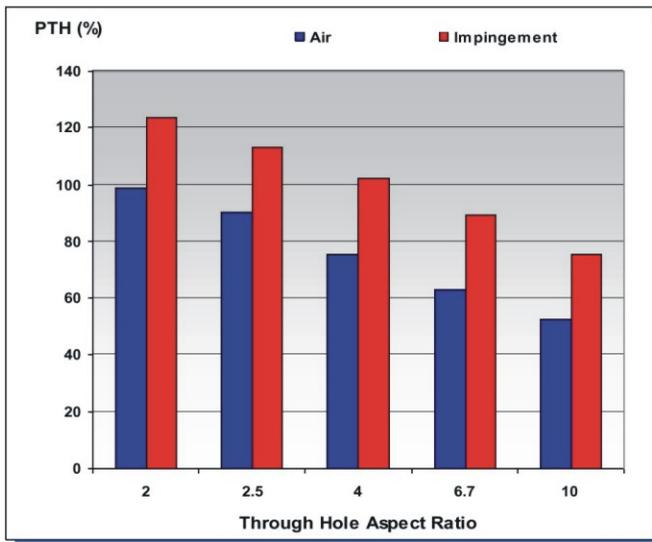


Figure 6. PTH Throwing Power results

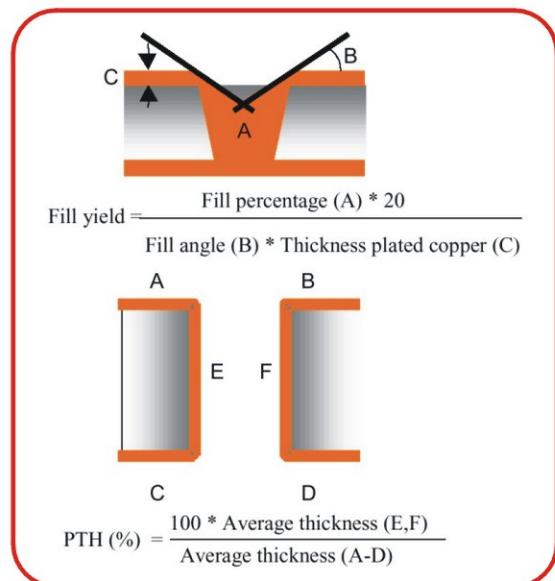


Figure 7. Viafill and PTH efficiency

microvia base, further improving the "bottom-up" via-fill efficiency and eliminating any cavities. Under such conditions, the through holes can also be plated with good throwing power⁷ (e.g. 5:1 AR plating at 80-85% throwing power using a three point measurement method for the hole wall vs. surface thickness. These are shown in Figure 6.

Definition of via filling efficiency and through-hole plating efficiency

The Via Fill Yields (VFY) and through hole metallization (PTH) metrics are calculated as shown in Figure 7. The VFY takes into account not only the percentage of fill of the microvia, but also the thickness of the plated copper on top of the board and (in case of incomplete fill) the fill angle (B). The smaller this fill angle the easier it will be to fill the microvia with solder or resin without

entrapment of air. Typically yield values over 5% represent good fill. For the through holes, the objective is usually PTH > 80% based on the three point method of measurement.

Some typical via-fill profiles are shown in figure 8. As illustrated, the solderable surfaces of the pads no longer have deep wells to trap air. Limiting the contribution of the microvia to solder joint void formation has been the topic of many studies, and there are several methods available to minimize the microvia's contribution.

Published Studies on Microvia Voiding

Several earlier studies on microvias and voiding have been published previously in 2003.^{3,4,5} and have shown, among other findings, that copper-filled microvias exhibited the best results in reducing voiding. Vias that were completely filled showed less voiding than vias that were partially filled, presumably because less entrapped air creates less voids. Smaller via sizes were seen to create smaller voids than larger vias. And on the assembly side, IR soak profiles produced less voids than ramp profiles. These studies were performed prior to the introduction of low voiding solder paste formulations.

Over 2004-2006 a further major investigation was undertaken which applied the simple 2-step Copper Via Fill technique previously described. This study examined the influence of: via presence and size; tin-lead and lead-free (SAC305) alloy systems; PWB solderable finish type and the impact of copper blind microvia filling vs. unfilled (100 and 150 microns diameter). The complete report of the study⁶ can be obtained from the Surface Mount Technology Association web site (smta.org). A summary of some of the findings from study included:

- Fewest voids were produced on pads with no vias at all, more were produced on pads with 4 mil unfilled vias, and the most were produced on pads with unfilled 6 mil vias.
- The lead-free system performed equivalently or slightly better with respect to void production. This is an important fact to note, because for

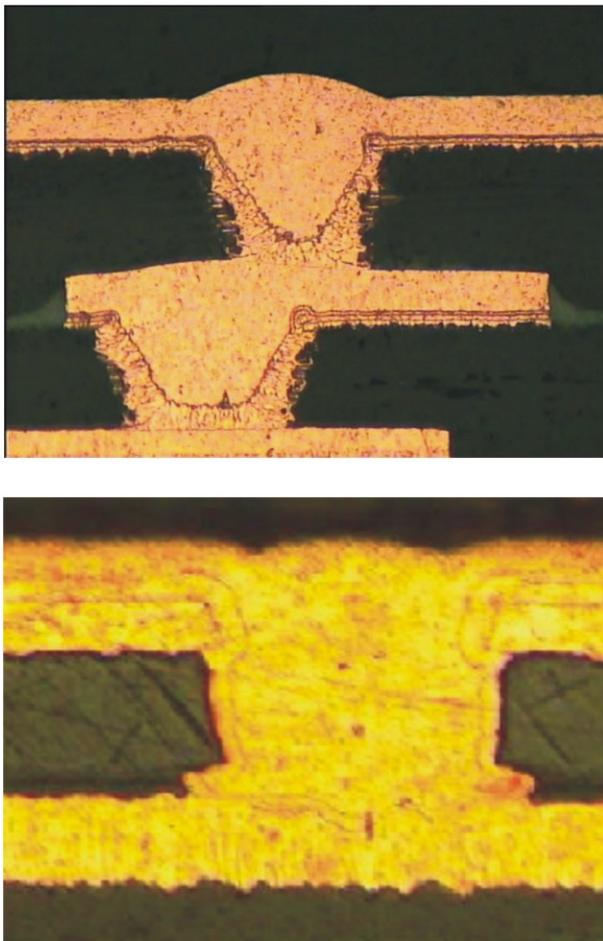


Figure 8. Some typical via-fill results from the 2-step system

many years lead-free solder pastes were believed to produce more voids than tin-lead.

- Of the three surface finishes included, both OSP and ImAg generally produced similar amounts of voids, which were less frequent and smaller than those produced with ENIG finish.
- **Effect of Via Filling** - The most remarkable result was the effect of filling the vias with copper. The investigators found it impossible to differentiate the voiding performance between filled vias and pads with no vias at all, regardless of device type or alloy system. The charts in figures 9 and 10 show the voiding behavior of 0.8mm FlexBGA devices.

As shown here, it is easy to visually differentiate the performance of the unfilled vias from the other two test conditions. But it is not so easy to discern a performance difference between the pads without vias and the ones which had the vias filled. The data from these two conditions were analyzed statistically, and it was determined that with 95% statistical significance, the voiding rates produced on pads with filled microvias are equal to the voiding rates produced on pads with no vias at all. With filled microvias there is no room for air to get trapped during the printing process, thus no contribution from the microvia to solder void production, and no concerns regarding void location based on final finish.

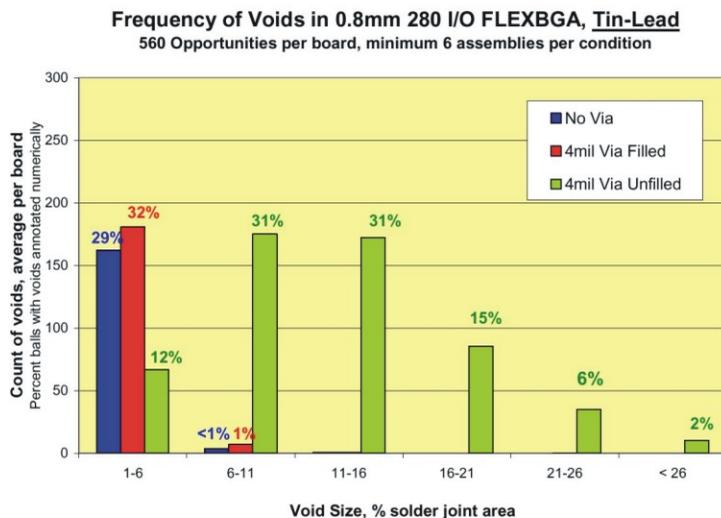


Figure 9. Voiding comparison of pads with no vias, pads with filled vias, and pads with unfilled vias soldered with tin-lead solder paste.

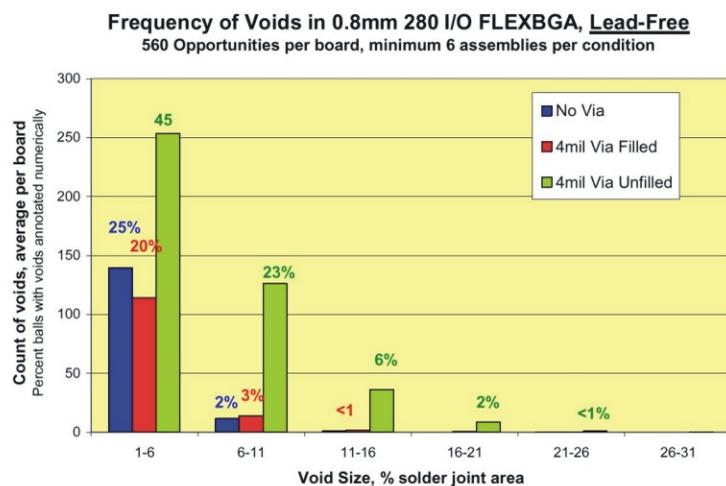


Figure 10. Similar comparison on jointed soldered with lead-free solder paste.

Conclusions

HDI and microvia-in-pad technologies continue to facilitate the development of smaller, lighter, more powerful electronics by enabling finer pitch I/O's, thinner circuit boards, and higher routing densities. In concert with this, HDI and microvia-in-pad technology is becoming much more prominent within the design, fabrication and assembly of new products regardless of the end segment technology or device served.

Several fabricators have already embraced the application of Copper ViaFill and now provide volume product to this type of specification. Others are only just facing the hurdles of implementation and looking how best to address the additional process steps and cost adders. For assemblers, those hurdles included solder joint starving; solder joint voiding and overall reliability concerns for the end product. The good news is that many of these concerns have been addressed, and a numerous methods of resolution are available.

The specific solution of filling the vias with copper plating in the same process as PTH plating directly addresses these needs in

three ways: it provides better thermal and electrical design characteristics compared to existing technologies, it reduces process steps in fabrication, and it eliminates excessive voiding in board-level assembly. And it does it all within relatively short plating times while offering simplified and consistent methods of process control. Given that the major obstacles have been cleared, a broad spectrum of electronics sectors can now employ HDI and microvia-in-pad technologies and enjoy the cost and performance benefits that they bring to the end product.

Acknowledgement

The most recent study cited above was a two-year endeavor, and this article incorporates some key findings of this activity. Many thanks to the many contributors to the study: Chrys Shea, Rahul Raut and Lou Picchione of Cookson Electronics, Quyen Chu and Nicholas Tokotch of Jabil Circuit, and Dr. Paul Wang of Microsoft.

References

1. Japanese patent application JP20002 19994(A); European patent application EP1152071A1
2. IPC-6012B, Qualification and Performance Specification for Rigid Printed Boards, IPC, Bannockburn, IL, 2007
3. Grano, F, et al, "Impact of Micro-Via in Pad Design on Void Formation," Proceedings of SMTA International, September, 2003
4. Harjinder, L. and Sundar, S, "Assembly Issues with Microvia Technologies," Proceedings of SMTA International, September, 2003
5. Singer, et al, "The Effect of Via-In-Pad Via Fill on Solder Joint Void Formation," Proceedings of IPC Works, October, 2003
6. Shea, et al, "BGA Solder Void Correlation to Via-In-Pad, Via Fill, Surface Finish, and Lead-Free Solder Final Report," Proceedings of the Pan Pacific Microelectronics Symposium, January, 2007
7. "Simultaneous Microvia Filling and Through-Hole Metallization", A.Lachowicz et al CPCA proceedings March 2006
8. H.Verbunt, D. Isik, U. Schmergel, Dr. J. Rasmussen: "Optimized Vertical Process for

Microvia Filling and Through Hole Metallization under Production-like Conditions", IPC, Anaheim, Feb. 2005)